AGGIOS Seedlings
Power Reference Designs:
Xilinx Zynq UltraScale+ MPSoC

Whitepaper

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Executive Summary

AGGIOS' patented Software Defined Energy Management products deliver unprecedented power savings while preserving full functionality for a wide range of electronic devices in aerospace & defense, automotive, industrial, consumer, and data center applications. Typical power savings range from 30% to 60% delivering radical feature improvements for battery-operated, thermally-sensitive or energy-constraint devices. AGGIOS products act exclusively through automated system software and firmware optimizations without costly and time-consuming modifications to the original hardware or applications software. The result are longer lasting, cooler and smaller electronic devices delivered on schedule at fraction of costs. The reduction of power allows improvements of power-hungry advanced artificial intelligence and deep learning algorithms for edge devices while preserving battery-life and thermal characteristics.

Device designers use AGGIOS EnergyLab IDE on their development workstations to simulate power what-if scenarios of the complete device, configure the power management and conduct power measurements on the prototyping or custom production board. AGGIOS Seed Power Manager is a configurable embedded software stack loaded on the target device that monitors and controls power of the SoC and board. Designers select Seed optimizations and evaluate options in verification runs using the EnergyLab power measurement capabilities. The EnergyLab tool and the Seed Power Manager offer optimum power results, shorter time-to-market and provide high flexibility for trade off choices for custom boards and applications.

For designs relying on standard prototyping boards and applications, AGGIOS offers Seedling Power Reference Designs as the shortest, lowest cost path to fully optimized designs. Seedlings come with the Seed Power Manager preconfigured with a set of power optimization options for selected standard boards and applications and the EnergyLab test and measurement tool for power verification.

This whitepaper presents detailed measurements of six Seedling Power Reference Designs for standard Xilinx Zynq UltraScale+ MPSoC evaluation boards and reference applications. The achieved power consumption and savings are compared to respective original reference designs intended to demonstrate technologies using default power management as summarized in the table below.

Application	Description	SoC Version	Board	Mode	Xilinx TRD or equivalent	AGGIOS PRD	Difference	Saved
Video	1080p60 streaming	ZU7EV	ZCU106	Active PS and PL	4,559 mW	2,950 mW	- 1,609 mW	35%
Video	Deep Learning - Region of Interest	ZU7EV	ZCU106	Active PS and PL	10,959 mW	4,201 mW	- 6,758 mW	62%
ECC	ECC processing	ZU9EG	ZCU102	Active PS and PL	3,702 mW	1,573 mW	- 2,129 mW	58%
Benchmark	Memory throughput	ZU9EG	ZCU102	Active PS only	1,714 mW	1,031 mW	- 683 mW	40%
SDR	Radio	ZU9EG	ZCU102	Signal Detection APU/Linux only	1,680 mW	535 mW	- 1,145 mW	68%
SDR	Radio	ZU9EG	ZCU102	Signal Detection RPU/RTOS only	350 mW	50 mW	- 300 mW	86%

For the first three application cases listed above, that deliver power savings of 35%, 62% and 58% respectively, the Seed Power Manager optimizes power of both the Zynq UltraScale+ MPSoC processing system containing ARM cores and the programmable logic. In the remaining cases the programmable logic portion is turned off and power gains are resulting from the processing system portion only and still deliver power savings of 40%, 68% and 86% respectively. Functional equivalence of the improved and original designs is verified on test runs using real-life settings.

None of the applied Seed Power Manager power optimizations are bound to the features of the Xilinx product line, the selected SoCs or the presence or absence of ARM cores or programmable logic, or particular board features. For that reason, we believe the same techniques can be applied and similar power improvements achieved for SoC and FPGA products of other semiconductor manufacturers.

For detailed videos please visit: https://www.youtube.com/channel/UCHaOy23ETlImizuAyHIHd2Q

1 Introduction

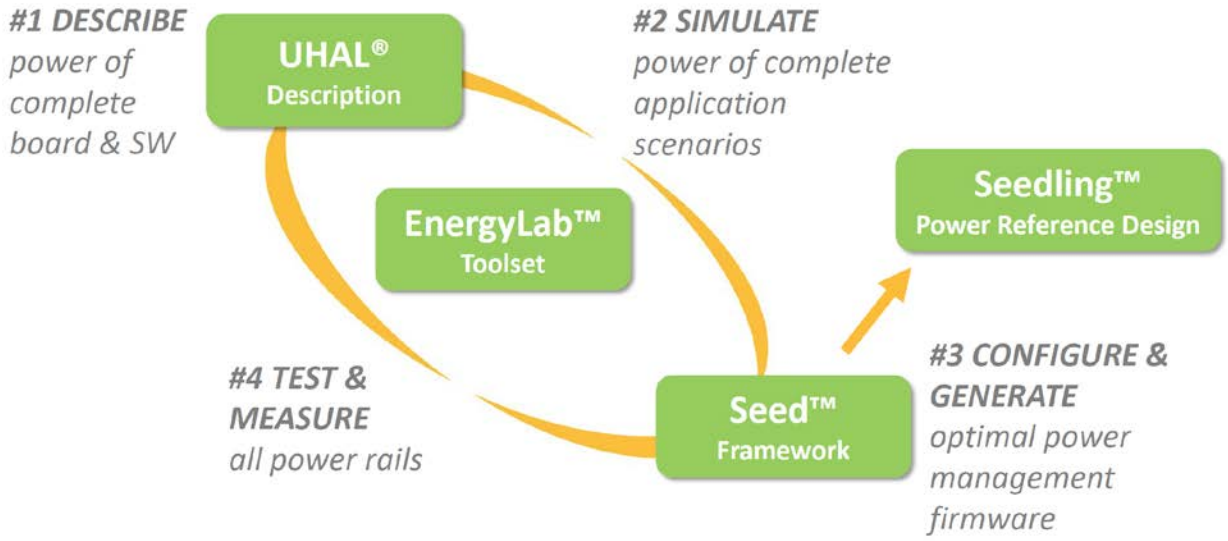
AGGIOS Seedlings™ Power Reference Designs (PRDs) are complete applications optimized for power and thermal behavior while preserving full functionality. Based on the AGGIOS Seed™ power manager, Seedlings reduce time-to-market and development costs by providing comprehensive solutions for out-of-the-box implementation of standard applications on commercially available boards. Seedlings are delivered with pre-configured Seed power management software and the EnergyLab™ test & measurement tool for verification of power and thermal characteristics of the application.

This white paper presents power measurement results for Seedlings of Xilinx Zynq UltraScale+ MPSoCs using Xilinx Targeted Reference Design (TRDs) and other reference applications. For comparison, power measurements are also provided for the original non-optimized reference designs.

1.1 AGGIOS Seed Manager and EnergyLab Tool

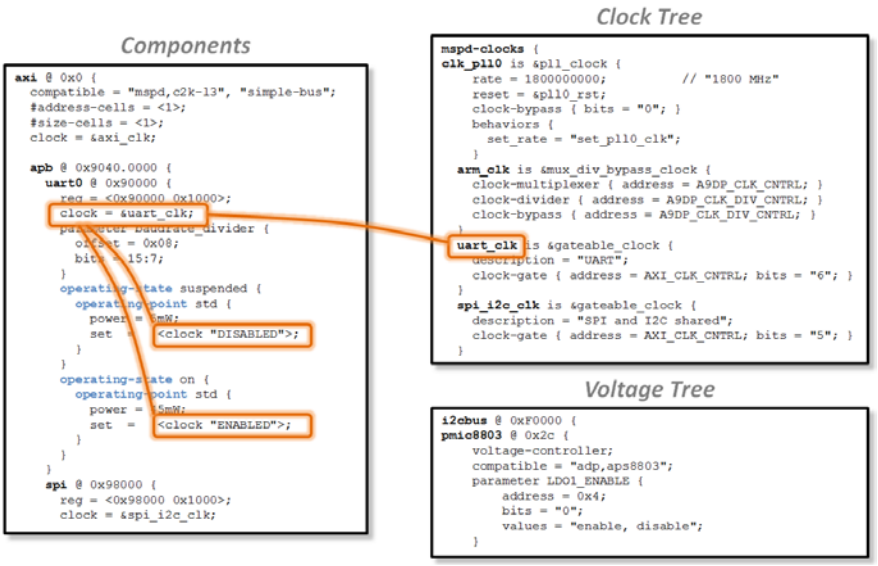
AGGIOS Seed Manager enables run-time management of power, energy, latency and thermal characteristics of complete applications running on heterogeneous multi-core, multi-OS SoCs and FPGAs. The Seed software drivers and firmware kernel complement the standard OSes or bare metal applications and take full control over platform power and thermal management to deliver advanced optimizations.

AGGIOS EnergyLab Tool allows users to (i) describe and simulate power of complete application scenarios including the applications and systems software, (ii) configure the Seed Manager for optimal power and thermal management, and (iii) provide runtime monitoring and analysis of the energy profile and power state details using real-time measurements on the target.



Seed configuration as well as EnergyLab simulation is driven by a UHA (Unified Hardware Abstraction) description of the system. A UHA model describes the programmer's view of the system focusing on power related details of all components which are controllable through software, either directly (direct access of registers through memory mapping or via GPIO/EMIO) or indirectly (access via intermediary components such as I2C controllers). UHA models also cover the software and its influences on component and system states and typically consist of library components as well as user defined components. Library components include the SoCs and a variety of board components, such as PMICs and memories. Application specific components, e.g. custom FPGA components or board level peripherals are described by the user, based on power estimates from data sheets or measurements on the target.

In order to allow accurate simulations as well as efficient power state management the UHA models also describe the dependencies between different components, expressed through references within component states, including clock, reset, and voltage dependencies.



For more information on UHA, Seed, Seedlings and EnergyLab, please consult: www.aggios.com/#products.

1.2 Xilinx UltraScale+ SoCs and Boards

Xilinx UltraScale+ SoC products allow hardware and software programmability for application development across a wide span of industries and technologies. The programmable logic (PL) hardware in the UltraScale+ Virtex and Kintex products line is complemented by the processing system (PS) in the UltraScale+ Zynq line of products allowing full software programmability. The results presented in this whitepaper were obtained through measurements on the Xilinx ZCU102 and ZCU106 boards.

The ZCU102 Evaluation Kit enables designers to jumpstart designs for automotive, industrial, video, and communications applications. This kit features the ZU9EG Zynq® UltraScale+™ MPSoC with a quad-core Arm® Cortex®-A53, dual-core Cortex-R5F real-time processors, and a Mali™-400 MP2 graphics processing unit based on Xilinx's 16nm FinFET+ programmable logic fabric. The ZCU102 supports all major peripherals and interfaces, enabling development for a wide range of applications. The ZCU106 development board features a Zynq® UltraScale+™ MPSoC ZU7EV device additionally equipped with a 4Kp60 capable H.264/H.265 video codec unit.

For more information on UltraScale+ devices and boards, please consult: www.xilinx.com

2 Measuring Power on Xilinx Boards

Many of the Zynq UltraScale+ MPSoC evaluation boards feature dedicated TI INA226 current and power monitors for each of the supply voltage rails of the SoC. An MSP430 microcontroller enables external I2C access to those power monitors via a UART interface. AGGIOS EnergyLab includes support for I2C based communication for a variety of ZCU1xx boards allowing to retrieve the power measurements and plot the measured results and display power state information in the Seed Monitor UI.

2.1 SoC Voltage Rails on the ZCU102 and ZCU106 Evaluation Boards

Power measurements are obtained via I2C communication with the INA226 power monitors for each of the rails. A table of the measured rails and their respective power domains is shown below:

Voltage rail	Power Domain	Shunt Size
VCC_PSINTFP	FPD	2 mOhm
MGTRA_VCC	FPD	5 mOhm
MGTRA_VTT	FPD	5 mOhm
VCCO_PSDDR_504	FPD	5 mOhm
VCC_PSDDRPLL	FPD	5 mOhm
VCC_PSINTLP	LPD	5 mOhm
VCC_PSAUX	LPD	5 mOhm
VCC_PSPLL	LPD	5 mOhm
VCC_OPS	LPD	5 mOhm
VCC_OPS3	LPD	5 mOhm

Voltage rail	Power Domain	Shunt Size
VCC_INT	PLD	5 mOhm
VCC_BRAM	PLD	5 mOhm
VCC_AUX	PLD	5 mOhm
VCC_1V2	PLD	5 mOhm
VCC_3V3	PLD	5 mOhm
MGTA_VCC	PLD	5 mOhm
MGTA_VTT	PLD	5 mOhm
VCC_VCU (*ZU7EV only*)	PLD	2 mOhm

The Zynq UltraScale+ MPSoC power domains of interest are (i) the low power domain (LPD) containing the low power peripherals and the Cortex-R5F real time processors, (ii) the full power domain (FPD) featuring the Cortex-A53 application cores and the high-speed peripherals and (iii) the programmable logic domain (PLD) containing the programmable logic. More details about Zynq UltraScale+ MPSoC power domains can be found in: https://www.xilinx.com/support/documentation/white_papers/wp482-zu-pwr-perf.pdf

2.2 Measurement Accuracy and Sampling Rate

The power measurements are conducted by measuring the voltage drop across a shunt resistor to compute the current as well as by measuring the supply voltage. The TI INA226 devices use 16-bit A/D converters with an LSB of the shunt register of 2.5µV. The LSB of the bus voltage registers is 1.25mV.

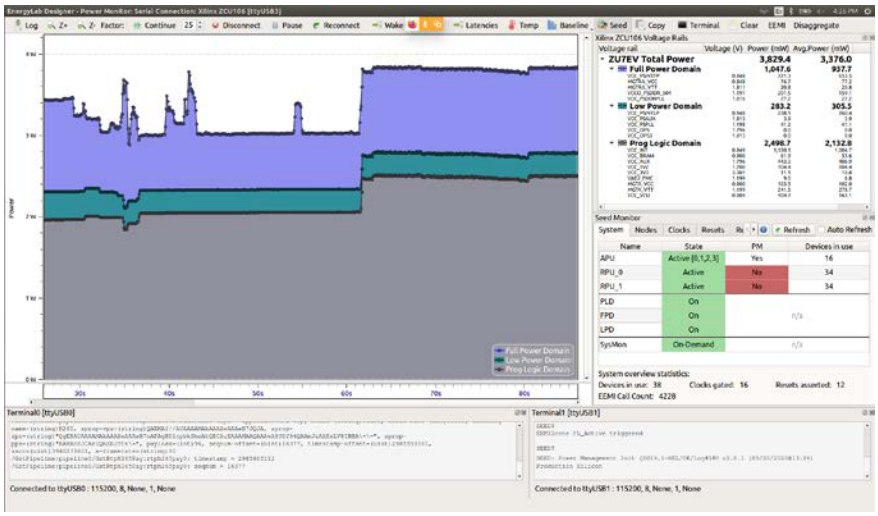
The sampling rate used is 10 samples per second. All measurements were obtained by averaging measurements over a period of 60 seconds, i.e. 600 samples for each measured voltage rail.

2.3 Temperature Measurements

The temperature of the Zynq UltraScale+ MPSoC is measured by Seed using on-chip telemetry and plotted in the EnergyLab IDE.

2.4 EnergyLab Power Measurements and Power State Analysis

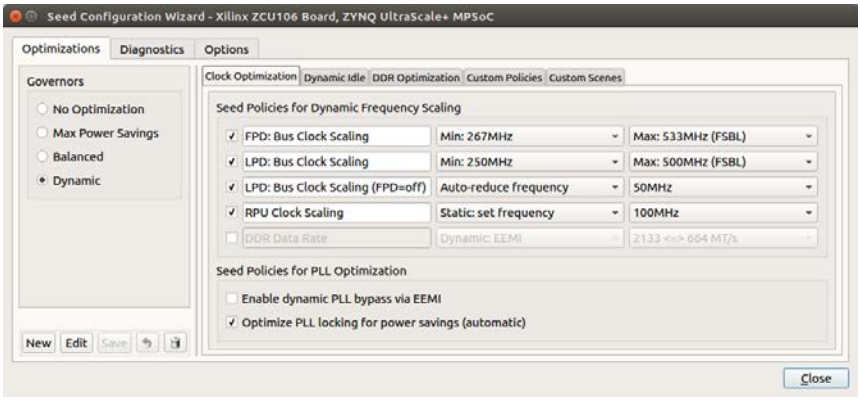
The EnergyLab IDE offers power measurement support on various Zynq UltraScale+ MPSoC boards, including the ZCU102/106 boards and Avnet's UltraZed and Ultra96-V2 boards. Measured power data is plotted in a graph, alongside the measured temperature. Additionally, EnergyLab features the Seed Monitor UI, which displays power state details for the system as well as individual components, clocks, and reset lines. The Seed Monitor UI is instrumental in identifying power optimization opportunities. An example of the Seed Monitor UI is shown below:



3 Optimizing Power with AGGIOS Seed and EnergyLab

AGGIOS Seed Manager enables run-time management of power, energy, latency and thermal characteristics for heterogeneous multi-core, multi-OS SoCs and complete applications. The Seed software drivers and firmware kernel complement the standard OSes and take full control over power and thermal management.

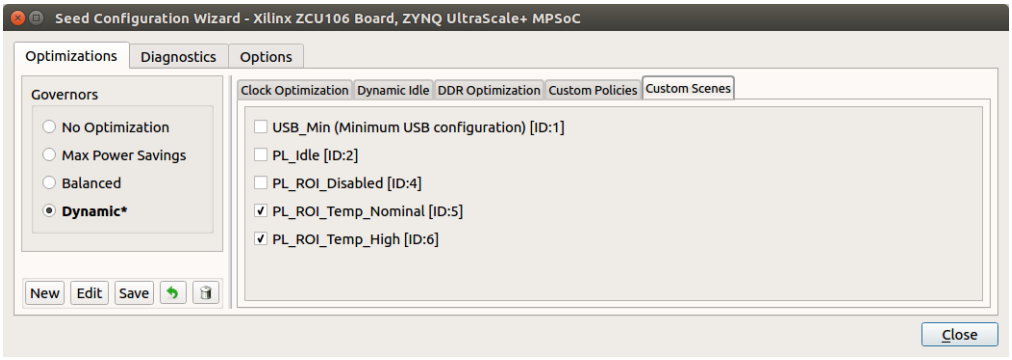
Seed can be configured from the EnergyLab Designer IDE allowing users to tune power and thermal management to fit their application. An example of the Seed Configuration Wizard for clock optimization is shown below:



Seed offers a variety of dynamic power optimization features, which can be customized using the AGGIOS EnergyLab IDE (see figure above). In the case of the Xilinx Zynq UltraScale+ MPSoC, Seed optimizations consist of pre-defined optimization options for the PS portion of the SoC, and additional custom scenes and policies which can also cover the programmable logic, i.e. the PL portion of the SoC. PS optimizations range from dynamic clock frequency scaling options and PLL optimization to dynamic device idling and DDR optimization.

One example of custom scenes used in Seed is the use case for region-of-interest tracking as described in section 0, where we have defined scenes to allow reacting to thermal events, i.e. lowering the power consumption of the PL when the junction temperature exceeds a defined threshold.

Seed also supports PMIC control via PM-Bus, allowing Seed to control voltage rails, e.g. to power down the PLD or FPD voltage rails when the PL isn't used or the APU is in a suspend-to-RAM state.



Additionally, Seed can be configured to provide diagnostic information useful for optimizing power of a target device. It can report temperatures, measure state transition latencies, as well as provide power state details for the entire system as well as individual components, including clock configuration and reset state.

Once Seed is configured, the Seed firmware can be generated, producing an ELF file ready to be included in the application's boot image.

In many Zynq UltraScale+ MPSoC applications the PL portion will be responsible for the majority of the overall power consumption. Reducing the power draw of the PL can be achieved by a variety of methods such as gating clocks of unused logic, reducing clock frequencies, scaling voltages, or by powering down the entire PL domain during prolonged periods of inactivity.

Using custom scenes and policies Seed can quickly be configured to cover PL power optimizations. The PL designs themselves may require small modifications in order to inject clock gating and frequency reduction capabilities. AGGIOS power reference designs already include the necessary provisions in the PL design to allow for optimized power management via Seed. Custom designs can easily be upgraded by inserting Seed driven clock control components in the clock path. The EnergyLab Designer IDE allows the creation of custom scenes to control the state of the PL clocks when needed. Additionally, the power state selection can be automated by defining custom policies, autonomously triggering power state transitions based on power or thermal events, such as selecting a lower-speed clock frequency when a temperature threshold is exceeded.

4 Seedling Power Reference Designs Based on Xilinx Video TRDs

The following sections describe the video related power reference designs as well as the results measured on a ZCU106 evaluation board. The designs are based on Xilinx Targeted Reference Designs (TRD) that demonstrate technologies and are selected according to customer requirements. The original TRDs do include the default Xilinx power management.

4.1 1080p60 Video Streaming Seedling

This use case is based on the optimized Xilinx Video Codec Unit (VCU) TRD module "Low Latency PS DDR NV12 HDMI Video Capture and Display" as described on the Xilinx Wiki:

https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/180649993/Zynq+UltraScale+MPSoC+VCU+TRD+2019.2+-+Xilinx+Low+Latency+PS+DDR+NV12+HDMI+Video+Capture+and+Display

This module enables capture of video from an HDMI Rx subsystem implemented in the PL. The video can be streamed-out through an Ethernet interface at ultra-low latencies using Sync IP.

The board is connected to a video source via HDMI, and to a PC via Ethernet. The PC is running the VLC media player configured to display the video stream received from the ZCU106 board. The HDMI source is producing a 1080p60 video signal, playing a 1080p YouTube video.

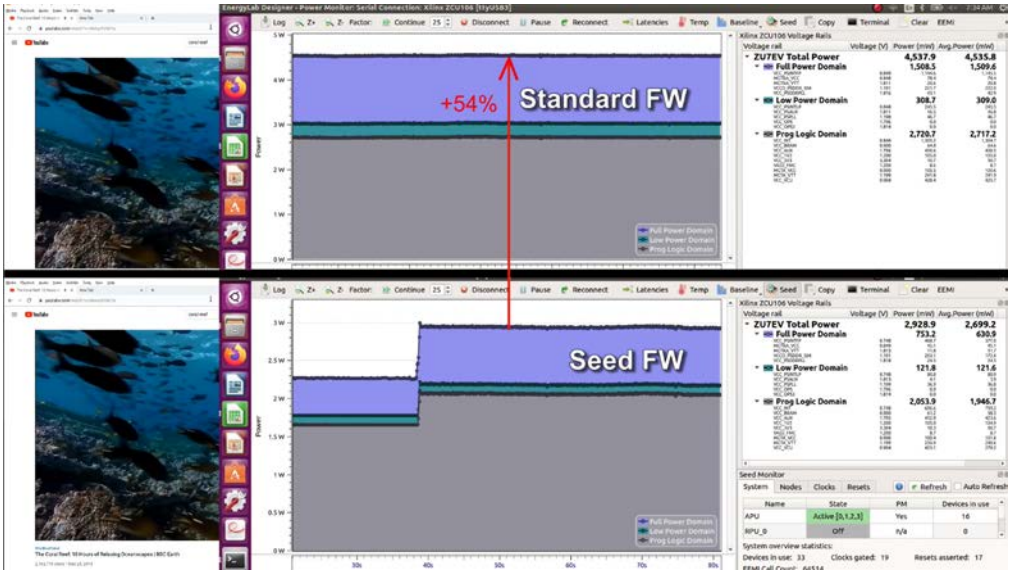
The power measurements of the PRD are shown in the table below. For comparison, we also show the measurements of the original Xilinx VCU TRD[1].

[1] VCU TRD version 2019.2

Voltage Rail	Power Domain	Seed Power Manager	Standard Power Manager	Savings	
VCC_PSINTFP	FPD	477.5 mW	1147.9 mW	670.4 mW	58%
MGTRA_VCC	FPD	45.1 mW	78.6 mW	33.5 mW	43%
MGTRA_VTT	FPD	11.7 mW	20.8 mW	9.1 mW	44%
VCCO_PSDDR_504	FPD	204.9 mW	220.8 mW	15.9 mW	7%
VCC_PSDDRPLL	FPD	24.5 mW	43.0 mW	18.5 mW	43%
VCC_PSINTLP	LPD	81.6 mW	246.2 mW	164.6 mW	67%
VCC_PSAUX	LPD	4.0 mW	16.7 mW	12.7 mW	76%
VCC_PSPLL	LPD	37.0 mW	46.7 mW	9.7 mW	21%
VCC_OPS	LPD	0.0 mW	0.0 mW	0.0 mW	0%
VCC_OPS3	LPD	0.0 mW	0.0 mW	0.0 mW	0%
VCC_INT	PLD	733.2 mW	1331.3 mW	598.1 mW	45%
VCC_BRAM	PLD	63.2 mW	65.8 mW	2.6 mW	4%
VCC_AUX	PLD	410.4 mW	449.0 mW	38.6 mW	9%
VCC_1V2	PLD	105.0 mW	105.0 mW	0.0 mW	0%
VCC_3V3	PLD	10.7 mW	10.5 mW	0.0 mW	0%
MGTA_VCC	PLD	98.5 mW	106.5 mW	8.0 mW	8%
MGTA_VTT	PLD	222.2 mW	243.5 mW	21.3 mW	9%
VCC_VCU	PLD	420.5 mW	426.5 mW	6.0 mW	1%
	Total	**2950.0 mW**	**4558.8 mW**	**1608.8 mW**	**35%**

The applied power optimizations have been verified to not impact the performance, i.e. the video is encoded with the exact same settings as defined in the original TRD and produces the same number of frames per second. A detailed demo of this Video Streaming Seedling can be found at:

https://www.youtube.com/watch?v=it0_3ccdy1c



The screenshot above shows the side by side comparison of the VCU reference design running with the standard firmware in the upper half and the Seed firmware below, with power measurements conducted using the EnergyLab IDE. In this case the penalty for not using the Seed Power Manager is a 54% higher power consumption.

4.2 VCU Region of Interest (ROI) Tracking Seedling

This reference design is based on the Xilinx Zynq UltraScale+ MPSoC Video Codec Unit (VCU) ROI design as described on the Xilinx Wiki:

https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/235602018/Zynq+UltraScale+MPSoC+VCU+ROI+2019.2

The primary goal of the VCU ROI design is to demonstrate the use of the DPU (Deep Learning Processor Unit) block for extracting the ROI (Region of Interest) from the input video frames and to use this information to perform ROI based encoding using the VCU encoder hard block present in Zynq UltraScale+ EV devices.

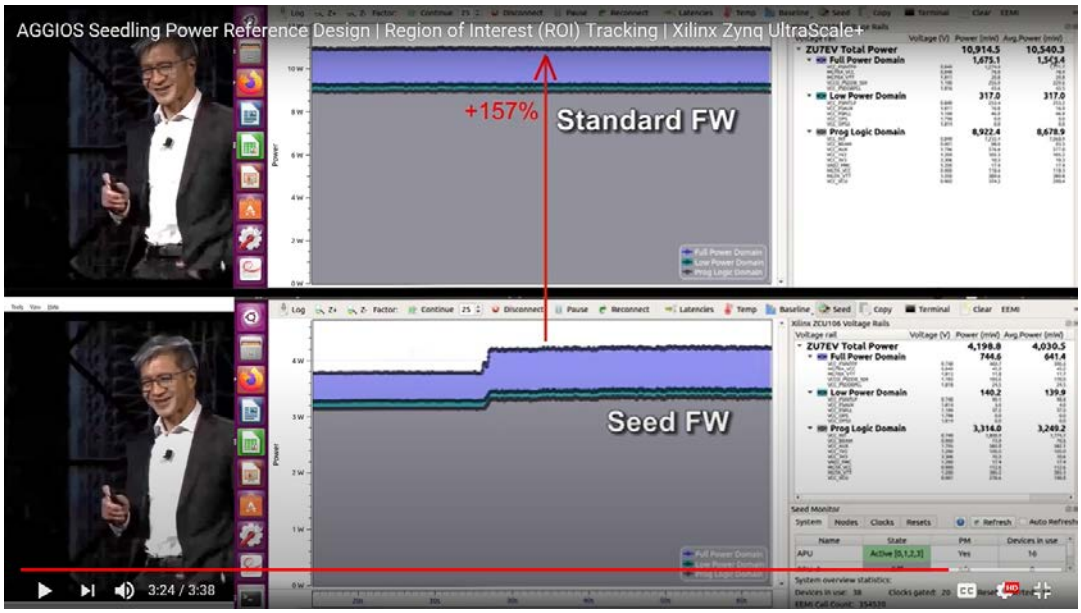
The design serves as a platform to accelerate Deep Neural Network inference algorithms using the DPU and demonstrate the ROI feature of the VCU encoder. The design uses a Deep Convolutional Neural Network (CNN) named Densebox, running on the DPU to extract ROI information, in this case faces.

The power measurement results are shown in the table below. To illustrate the effectiveness of the Seed Manager we've also conducted the same measurement using the standard power manager provided as part of the Xilinx SDK.

Voltage Rail	Power Domain	Standard Power Manager	AGGIOS Seed Power Manager	Savings	
VCC_PSINTFP	FPD	1202.6 mW	466.4 mW	736.2 mW	61%
MGTRA_VCC	FPD	79.3 mW	45.0 mW	34.3 mW	43%
MGTRA_VTT	FPD	20.8 mW	11.8 mW	9.0 mW	43%
VCCO_PSDDR_504	FPD	220.7 mW	192.1 mW	28.6 mW	13%
VCC_PSDDRPLL	FPD	43.5 mW	24.5 mW	19.0 mW	44%
VCC_PSINTLP	LPD	250.5 mW	99.0 mW	151.5 mW	60%
VCC_PSAUX	LPD	4.2 mW	3.9 mW	0.3 mW	7%
VCC_PSPLL	LPD	41.4 mW	37.2 mW	4.2 mW	10%
VCC_OPS	LPD	0.0 mW	0.0 mW	0.0 mW	0%
VCC_OPS3	LPD	0.0 mW	0.0 mW	0.0 mW	0%
VCC_INT	PLD	7386.7 mW	1825.1 mW	5561.6 mW	75%
VCC_BRAM	PLD	101.0 mW	74.7 mW	26.3 mW	26%
VCC_AUX	PLD	588.5 mW	581.8 mW	6.7 mW	1%
VCC_1V2	PLD	105.3 mW	105.0 mW	0.3 mW	0%
VCC_3V3	PLD	10.4 mW	10.4 mW	0.0 mW	0%
MGTA_VCC	PLD	120.5 mW	113.0 mW	7.5 mW	6%
MGTA_VTT	PLD	389.9 mW	385.4 mW	4.5 mW	1%
VCC_VCU	PLD	393.8 mW	226.2 mW	167.6 mW	43%
	Total	**10959.1 mW**	**4201.5 mW**	**6757.6 mW**	**62%**

As in the previous use case, the selected power optimizations have been verified to not be impacting the performance. A detailed demo of this Video ROI Seedling can be found at:

https://www.youtube.com/watch?v=-zQCSgrBknc



The screenshot above shows the side by side comparison of the original ROI reference design running with the standard firmware in the upper half and the optimized Seedling version below, with power measurements done using the EnergyLab IDE. In this case the penalty for not using the Seed Power Manager is 157%.

5 Other Seedling Power Reference Designs

This chapter highlights other use cases where power has been optimized using the AGGIOS Seed Manager, for each showing the measured power consumption of the original design and the optimized version using Seed.

5.1 Error Correcting Coding Seedling

This design is based on the Xilinx power advantage PL design on the Xilinx ZCU102 development board:

https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/18842217/Zynq+UltraScale+MPSoC+Power+Advantage+Tool+part+5+-+Building+and+Running+the+PL+Design+From+Sources

In order to allow optimizing the power consumption of the design we have added custom scenes to allow controlling both clock gating and clock scaling in the PL. Additionally, the PS power consumption has been optimized by selecting the "maximum power savings" governor for Seed which enables all available PS optimizations. The results are summarized in the table below.

Voltage Rail	Power Domain	Power Manager	AGGIOS Seed Power Manager	Savings	
VCC_PSINTFP	FPD	1088.9 mW	238.4 mW	850.5 mW	78%
MGTRA_VCC	FPD	82.9 mW	13.5 mW	69.4 mW	84%
MGTRA_VTT	FPD	28.7 mW	3.6 mW	25.1 mW	87%
VCCO_PSDDR_504	FPD	187.8 mW	161.7 mW	26.1 mW	14%
VCC_PSDDRPLL	FPD	44.7 mW	31.8 mW	12.9 mW	29%
VCC_PSINTLP	LPD	250.4 mW	61.5 mW	188.9 mW	75%
VCC_PSAUX	LPD	18.1 mW	6.3 mW	11.8 mW	65%
VCC_PSPLL	LPD	38.3 mW	24.2 mW	14.1 mW	37%
VCC_OPS	LPD	32.3 mW	15.0 mW	17.3 mW	54%
VCC_OPS3	LPD	0.9 mW	0.9 mW	0.0 mW	0%
VCC_INT	PLD	1318.0 mW	489.3 mW	828.7 mW	63%
VCC_BRAM	PLD	95.9 mW	28.2 mW	67.7 mW	71%
VCC_AUX	PLD	365.4 mW	365.2 mW	0.2 mW	0%
VCC_1V2	PLD	26.5 mW	26.5 mW	0.0 mW	0%
VCC_3V3	PLD	88.9 mW	72.3 mW	16.6 mW	19%
MGTA_VCC	PLD	12.7 mW	12.6 mW	0.1 mW	1%
MGTA_VTT	PLD	21.5 mW	21.5 mW	0.0 mW	0%
	Total	**3701.9 mW**	**1572.5 mW**	**2129.4 mW**	**58%**

The ECC functionality remains unchanged after the power optimizations with one out of the four ECC blocks running, at a quarter of the original clock speed (50MHz vs 200MHz).

5.2 Tinymem Benchmark Seedling

This use case highlights the power savings of optimizations in the DDR controller while running a dedicated memory benchmark on the main processors under PetaLinux and with the PLD powered off. The measurement results from the ZCU102 development board are summarized in the table below:

Voltage Rail	Power Domain	Standard Power Manager	AGGIOS Seed Power Manager	Savings	
VCC_PSINTFP	FPD	1089.6 mW	599.4 mW	490.2 mW	45%
MGTRA_VCC	FPD	61.6 mW	14.3 mW	47.3 mW	77%
MGTRA_VTT	FPD	19.8 mW	3.6 mW	16.2 mW	82%
VCCO_PSDDR_504	FPD	192.6 mW	215.3 mW	-22.7 mW	-12%
VCC_PSDDRPLL	FPD	52.5 mW	29.5 mW	23.0 mW	44%
VCC_PSINTLP	LPD	242.6 mW	139.5 mW	103.1 mW	42%
VCC_PSAUX	LPD	16.8 mW	4.0 mW	12.8 mW	76%
VCC_PSPLL	LPD	36.9 mW	24.5 mW	12.4 mW	34%
VCC_OPS	LPD	0.9 mW	0.9 mW	0.0 mW	0%
VCC_OPS3	LPD	0.9 mW	0.9 mW	0.0 mW	0%
	Total	**1714.2 mW**	**1031.9 mW**	**682.3 mW**	**40%**

Note that the results above are based on enabling of all available PS optimizations in the Seed configuration.

5.3 Software Defined Radio Seedling

This design demonstrates the use of low-power states for power sensitive applications.

The software defined radio application operates in different modes representing two different use case, one being the full interactive mode, the other being a background mode. Full interactive operation requires Linux running on the high-performance Cortex-A53 application processors (APU), whereas the background mode can be handled by the Cortex-R5F real-time processor (RPU), allowing the entire FPD domain to be turned off. In both use cases we enabled dynamic CPU and bus frequency scaling, PLL optimizations, as well as dynamic low power states for all unused peripherals and clocks, allowing the same applications to run at signifcantly reduced power levels. The interactive use case additionally benefited from Seed's optimizations of the DDR controller.

The table below shows the achieved results on a ZCU102 development board measured using the EnergyLab IDE:

Power Mode	Standard Power Manager	AGGIOS Seed Power Manager	Savings	
Signal Detection APU/Linux only	1680.0 mW	535.0 mW	1145.0 mW	68%
Signal Detection RPU/RTOS only	350.0 mW	50.0 mW	300.0 mW	86%

Using the Seed Manager there is no observable latency difference when compared to the standard Xilinx power manager. For full details of the Software Defined Radio use case please visit:

https://www.youtube.com/watch?v=e0QsneLgbP8

6 Summary

AGGIOS Software Defined Energy Management tools and software enable major reductions in power consumption for battery-powered, thermally-sensitive and energy-constrained electronic devices. The six real-life use cases presented in this white paper show a range of power savings from 35% to 86% compared to the original non-optimized designs with no impact on the functional performance of the application. The ROI use case has demonstrated a significant savings potential for designs with heavy use of programmable logic. For larger FPGAs we expect even higher power savings reaching high tens to hundreds of watts.

All power optimizations are automated and conducted solely by the device designers operating the AGGIOS tools and configurable software. No involvement of outside third parties is required, avoiding any exposure of devices' intellectual property or trade secrets.

AGGIOS products offer out of the box support for the components, boards and software of the following AGGIOS ecosystem partners:

XILINX	Zynq UltraScale+ MPSoC: ZCU102, ZCU106 Zynq UltraScale+ RFSoC: ZCU111 Virtex UltraScale(+) Kintex UltraScale(+) Zynq-7000 SoC: ZC702, ZC706
AVNET	Zynq UltraScale+ MPSoC: UltraZed, Ultra96 V2, UltraZed EV
infineon	IRPS5401 PMIC
NXP	i.MX 8QuadXPlus: MEK i.MX8M Mini: EVK i.MX7ULP: EVK
GENERAL DYNAMICS Mission Systems	OKL4 Hypervisor
Xen Project	Xen Hypervisor

Additional hardware and software support can be provided upon request. Detailed demonstrations of AGGIOS products can be found on the AGGIOS YouTube channel at:

https://www.youtube.com/channel/UCHaOy23ETlImizuAyHIHd2Q